PCI2390
User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART PCI2390 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART PCI2390 is a data acquisition module based on PCI bus. It can be directly inserted into IBM-PC/AT or a computer which is compatible with PCI2390 to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- PCI2390 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Digital Input

- Channel No.: 8
- Electrical Standard: TTL compatible
- High Voltage: ≧2V
- Low Voltage: ≦0.8V

Digital Output

- Channel No.: 8
- Electrical Standard: TTL compatible
- High Voltage: ≧2.4V
- Low Voltage: ≦0.5V
- Initial Power-on Value: Low level

Up/Backward Counter

- Channel No.: 8
- Resolution: 32-bit
- Counter Mode: UP_DWn controls, =1 is up counter, =0 is backward counter
- Count Mode: 6 modes (software selection)

- Electrical Standard: TTL compatible
- Gate (GATEn): Rising edge, falling edge, high level and low level
- Counter Output (OUTn): high level, low level
- Optical Isolation Voltage: 2500V
- Operating Temperature: 0℃~+50℃
- Storage Temperature: -20℃~70℃

Others

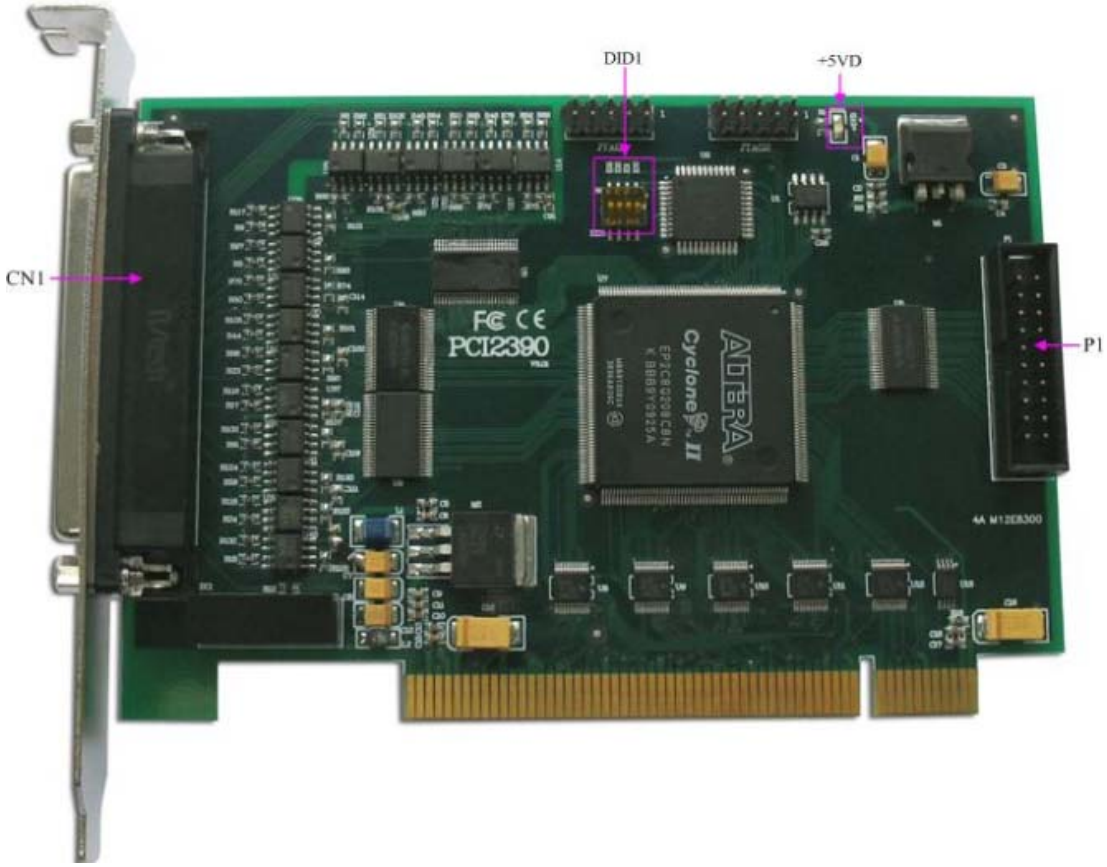
- Onboard Clock: 80MHz

Dimension

131mm (L) * 91.5mm (W)*16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



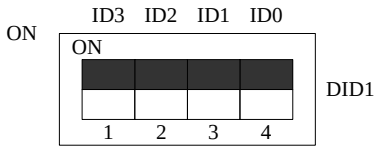
2.2 Signal Input/Output Connector

CN1: analog signal input connector

P1: digital input/output port

2.3 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one PCI2390 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-place numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: place "ID3" is the high bit."ID0" is the low bit, and the black part in the diagram represents the location of the switch. (Test software of the company often uses the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible. As for the differences between logic ID and physical ID, please refer to the function explanations of "CreateDevice" and "CreateDeviceEx" of ***The Prototype Explanation of Device Object Management Function*** in ***PCI2390S*** software specification).



The above chart shows"1111", so it means that the physical ID is 15.

The above chart shows"0111", so it means that the physical ID is 7.

The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

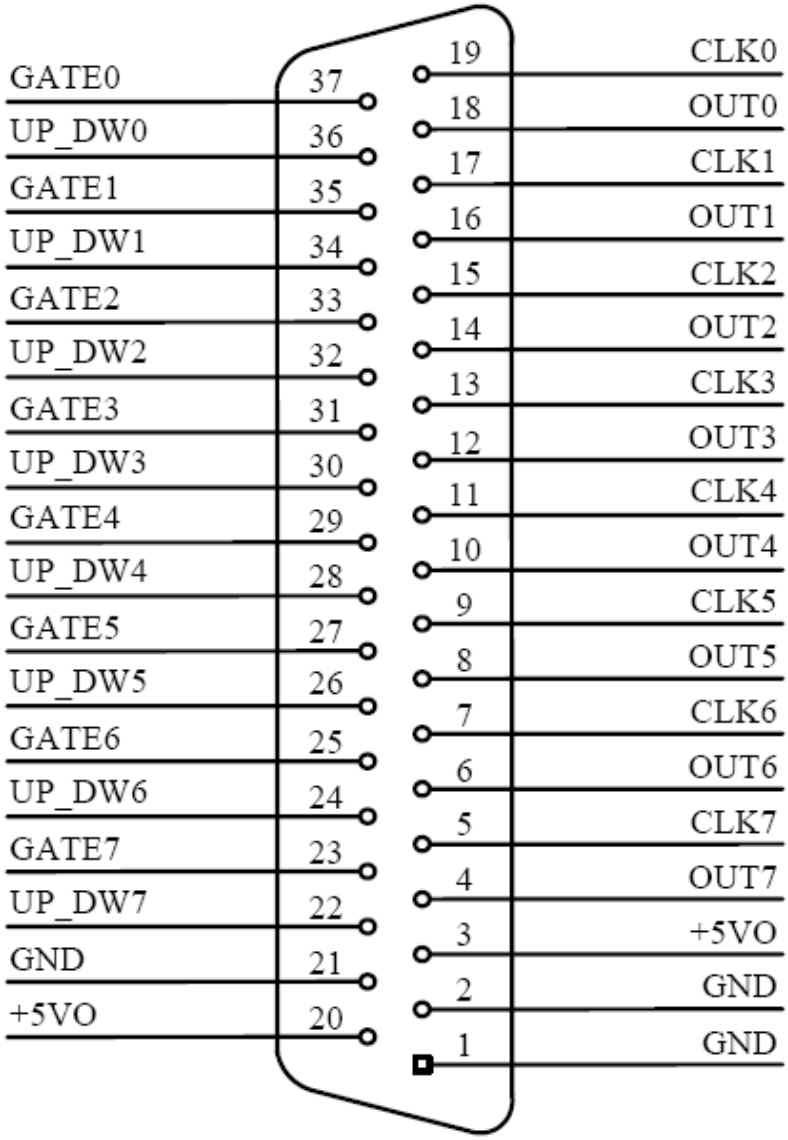
2.4 Indicator

+5VD: 5V power supply indicator, on for normal.

Chapter 3 Signal Connectors

3.1 The Definition of Signal Connector

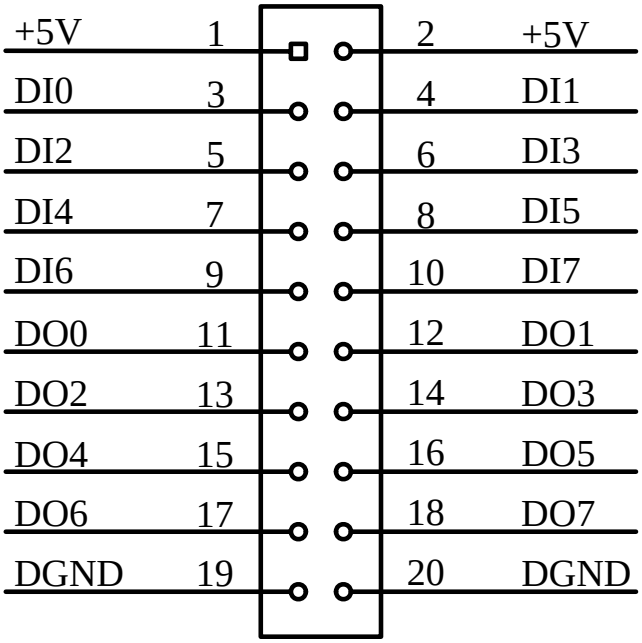
37 core plug on the CN1 pin definition



Signal Name	Type	Definition
CLK0~7	Input	Timer/counter clock source input.
GATE0~7	Input	Timer/counter input-gating.
OUT0~7	Output	Timer/Counter output.
UP_DW0~7	Input	Timer / counter count mode input, When UP_DW = 0, it is backward counter, when UP_DW = 1, it is up counter.
+5VO	Output	Output 5V power.
GND	GND	Counter signal ground.

3.2 The Definition of DI/DO Connector

20 core plug on the P1 pin definition



Signal Name	Type	Definition
DI0~DI7	Input	Digital input
DO0~DO7	Output	Digital output
+5V	PWR	5V power supply
DGND	GND	Digital ground

Chapter 4 Connection Ways for Each Signal

4.1 Digital Input Connection

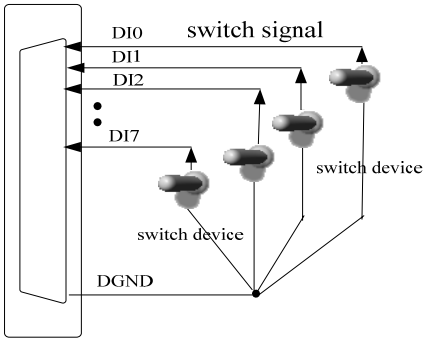


Figure 4.1 digital signal input connection

4.2 Digital Output Connection

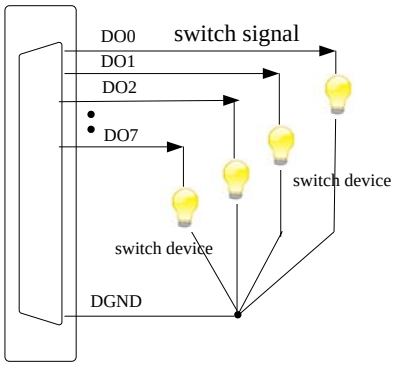


Figure 4.2 digital signal output connection

4.3 Timer/Counter Connection

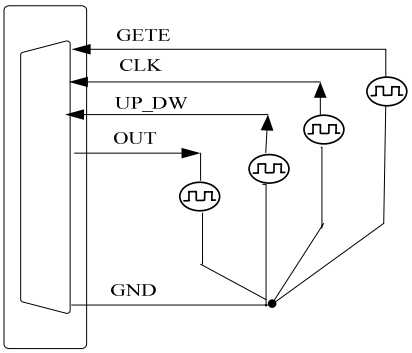


Figure4.3 Timer/counter connection

Chapter 5 Timer/Counter Function

5.1 Backward Counter

Mode 0: Interrupt on terminal count

In this mode, when the initial value assigned, if GATE is high level, the counter immediately to count by subtracting 1, and the output becomes low level. When the value turns to 0, the output becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter recount from the new initial value. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted.
Time diagram is shown in Figure 1.

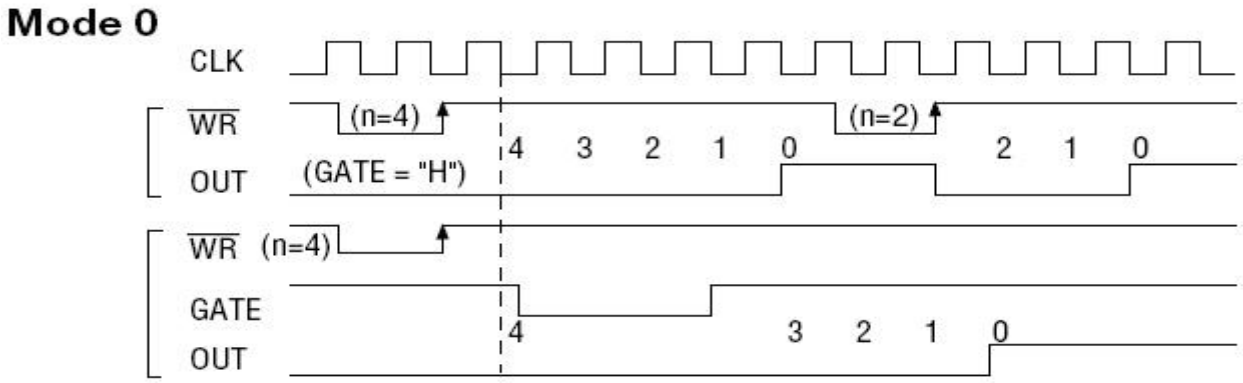


Figure 1

Mode 1: Hardware retriggerable ONE-SHOT

The mode can work under the role of GATE of gating signal. When given the initial value, OUT becomes high level, if “GATE” signal has a rising edge, the counter immediately begins to count, at this time the output OUT turns into low level. When the count ends, in other word, the count value turns to 0, the output OUT turns to high level, the output width of one-shot is deceived by initial value. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “0” and there is a “GATE” rising edge, the counter will begin to count from the new value. If there is a “GATE” rising edge when the counter is working, the current counting is stopped and re-start counting from the initial value. So the output single pulse has been widened
Time diagram is shown in Figure 2.

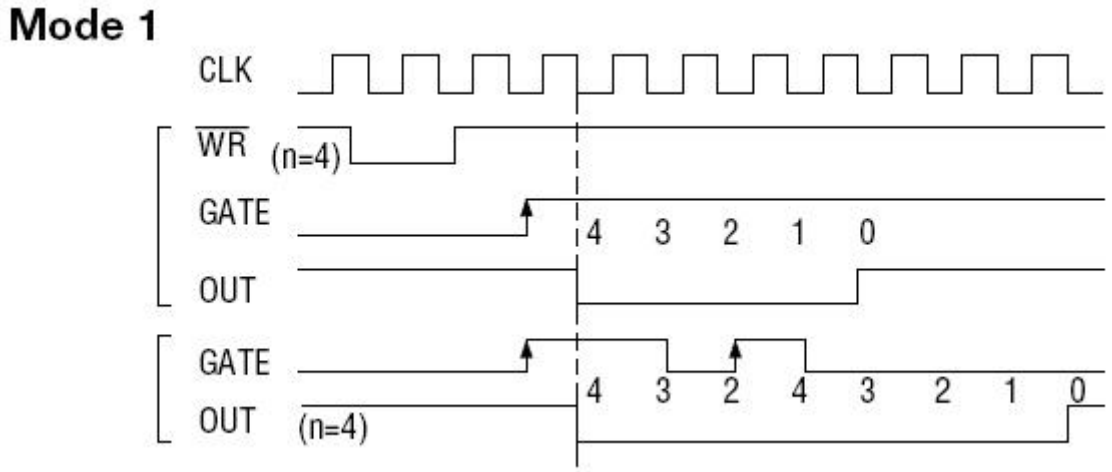


Figure 2

Mode 2: Rate Generator

Set this mode, the counter loads the initial value of n, start counting from the (n-1), OUT becomes high level, when the count value reaches 0, the OUT becomes low level. After a CLK cycle, OUT restore high level, and then the counter automatically load the initial value n, restart counting from the (n-1). Therefore, the output terminal will continue to output negative pulse, whose width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. Set a new initial value during a counting period, the counter start a new count cycle next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted.

Time diagram is shown in Figure 3.

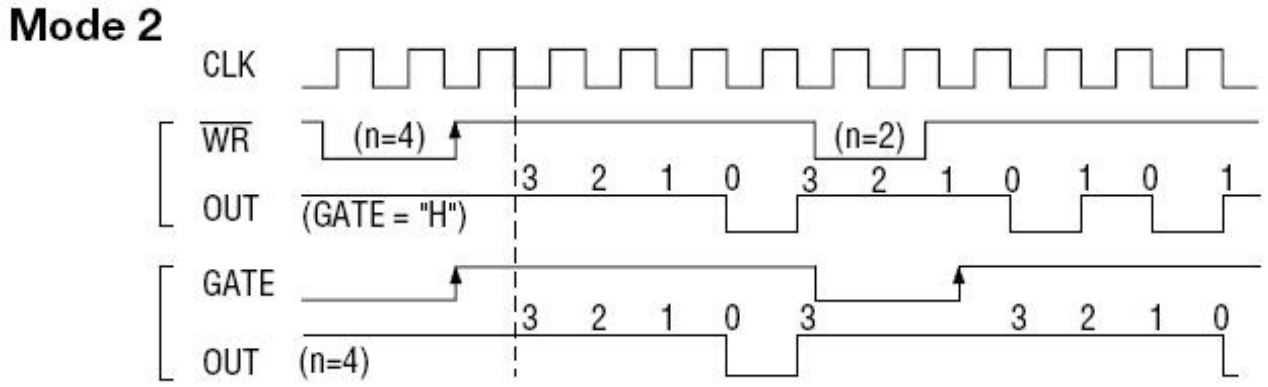


Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter loads the initial value of n, start counting from the (n-1) when the signal of GATE has a rising edge, timer/counter begins to count by subtracting “1” each time. The “OUT” terminal output high level when the count value is more than half of the initial count value, and it turn to low level when the count value is less than half of the initial value. If the initial count value n is an even number, then output 1:1 square wave, if the initial count value a is odd number, the output has remained high level during the previous (n +1)/2 count period, but the output becomes low level during the post (n-1) /2 count period, that is high level has one clock cycle than low level. Set a new initial value during a counting period, the counter start a new count cycle next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted.

Time diagram is shown in Figure 4.

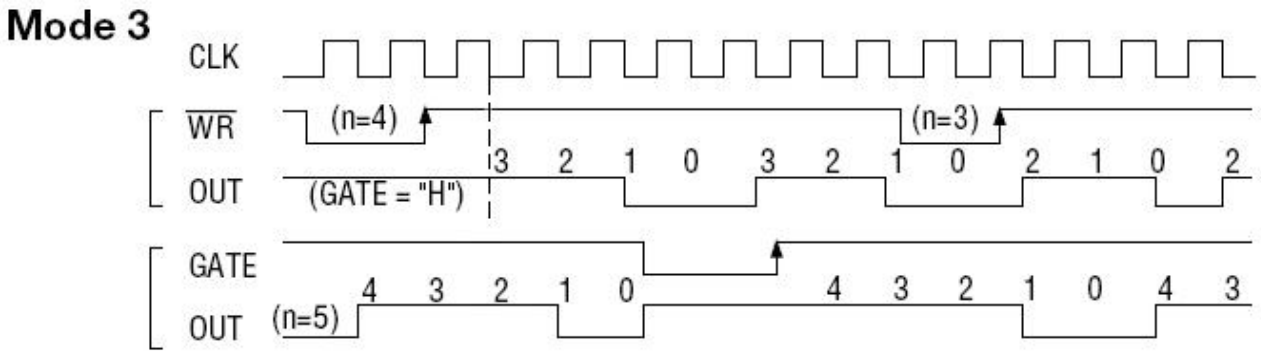


Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter starts counting after is given the initial value n, and OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted.

Time diagram is shown in figure 5.

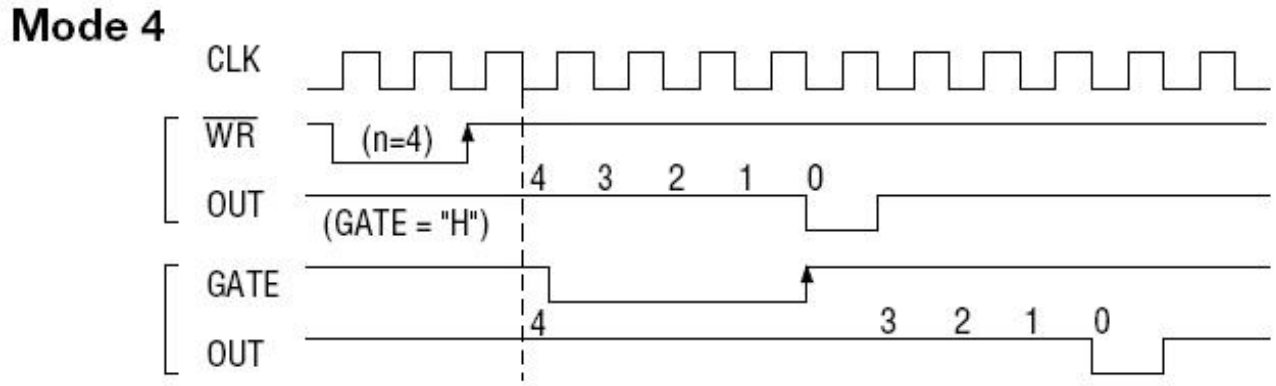


Figure 5

Mode 5: Software triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “0” and there is a “GATE” rising edge, the counter will begin to count from the new value.

Time diagram is shown in figure 6.

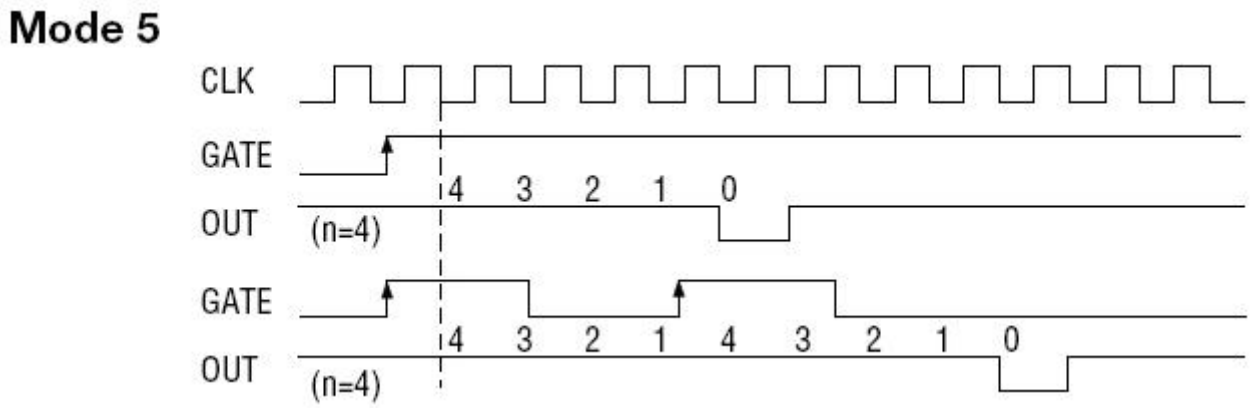


Figure 6

5.2 Up Counter

To facilitate the description, make M = 4294967295 = 2^{32}-1, the maximum count for the addition.
If the initial value is 4294967291, then recorded as (M-4), if it is 4294967292, then recorded as (M-3), and so on.

Mode 0: Interrupt on terminal count

In this mode, when the initial value assigned, if GATE is high level, the counter immediately to count by adding 1, and the output becomes low level. When the value turns to M, the output becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter recount from the new initial value. GATE=1 enables counting; GATE=0 disables counting.
Time diagram is shown in Figure 7.

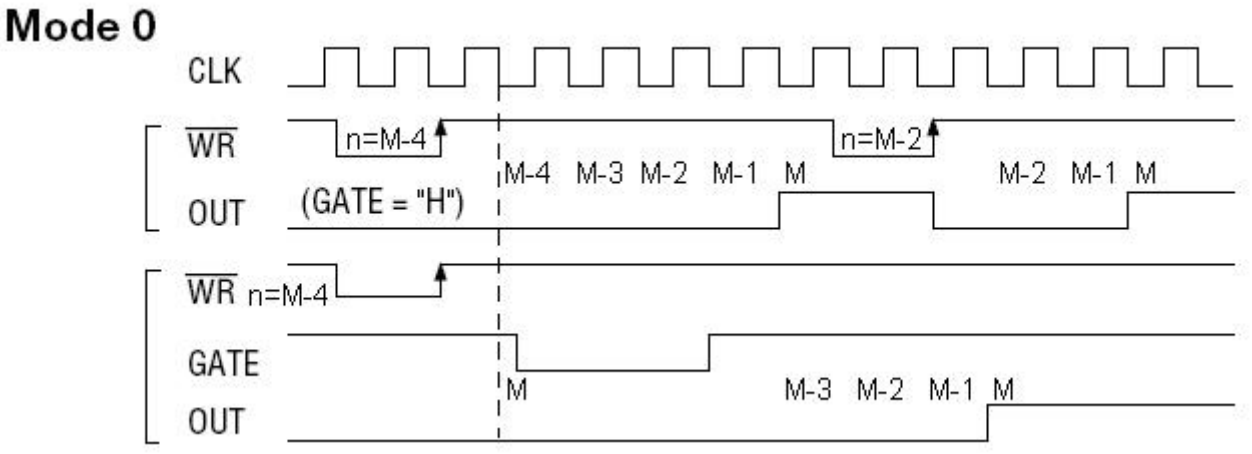


Figure 7

Mode 1: Hardware retriggerable ONE-SHOT

The mode can work under the role of GATE of gating signal. When given the initial value, OUT becomes high level, if “GATE” signal has a rising edge, the counter immediately begins to count, at this time the output OUT turns to low level. When the count ends, in other word, the count value turns to M, the output OUT becomes high level, the output width of one-shot is deceived by the difference between M and initial value n, that is M-n. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “M” and there is a “GATE” rising edge,

the counter will begin to count from the new value. If there is a “GATE” rising edge when the counter is working, the current counting is stopped and re-start counting from the initial value. So the output single pulse has been widened
Time diagram is shown in Figure 8.

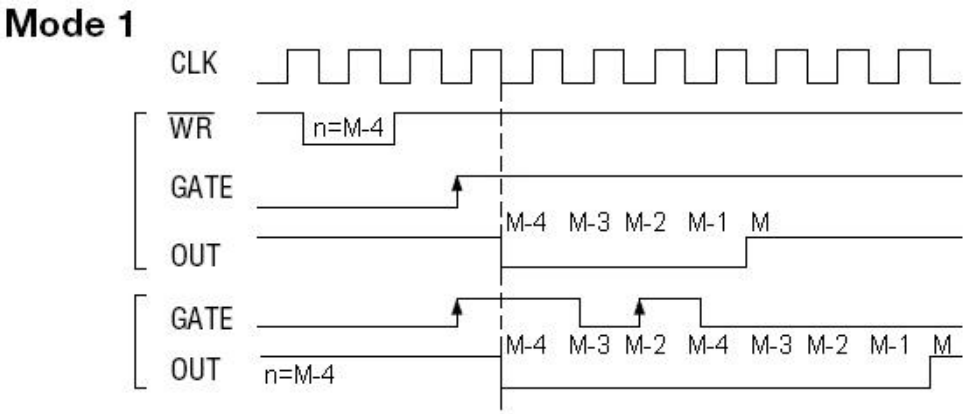


Figure 8

Mode 2: Rate Generator

Set this mode, the counter loads the initial value of n, start counting from the (n+1), OUT becomes high level, when the count value reaches M, the OUT becomes low level. After a CLK cycle, OUT restore high level, and then the counter automatically load the initial value n, restart counting from the (n+1). Therefore, the output terminal will continue to output negative pulse, whose width is equal to one clock cycle, the clock number between the two negative pulses is equal to the difference between M and initial value, that is M-n. Set a new initial value during a counting period, the counter start a new count cycle next time. GATE=1 enables counting; GATE=0 disables counting.
Time diagram is shown in Figure 9.

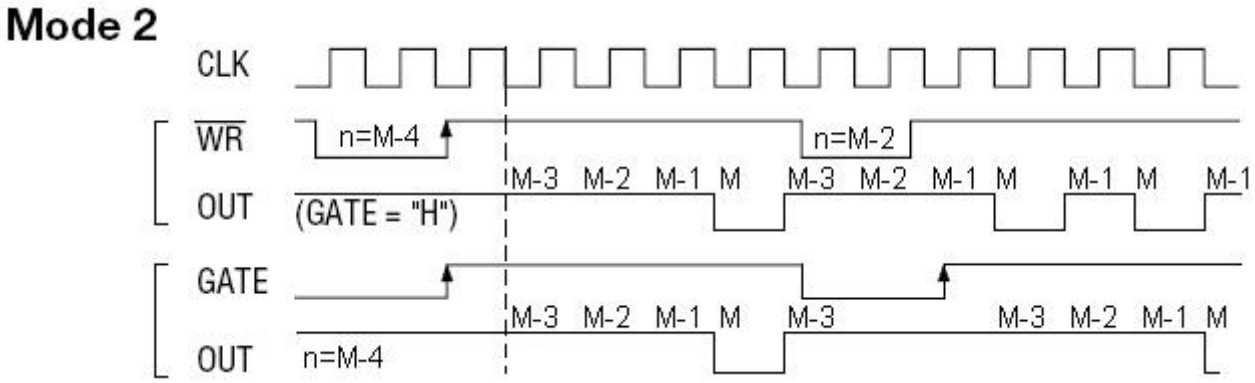


Figure 9

Mode 3: Square wave mode

Similar to Mode 2, the counter loads the initial value of n, start counting from the (n+1) when the signal of GATE has a rising edge, timer/counter begins to count by adding “1” each time. The “OUT” terminal output high level when the first half count is completed, and it turn to low level when carries out the second half count. If the initial count value n is an odd number, then output 1:1 square wave, if the initial count value a is even number, the output has remained high level during the previous (M-n +1)/2 count period, but the output becomes low level during the post (M-n-1) /2 count period, that is high level has one clock cycle than low level. Set a new initial value during a counting period, the counter start a new count cycle next time. GATE=1 enables counting; GATE=0 disables counting.

Time diagram is shown in Figure 10.

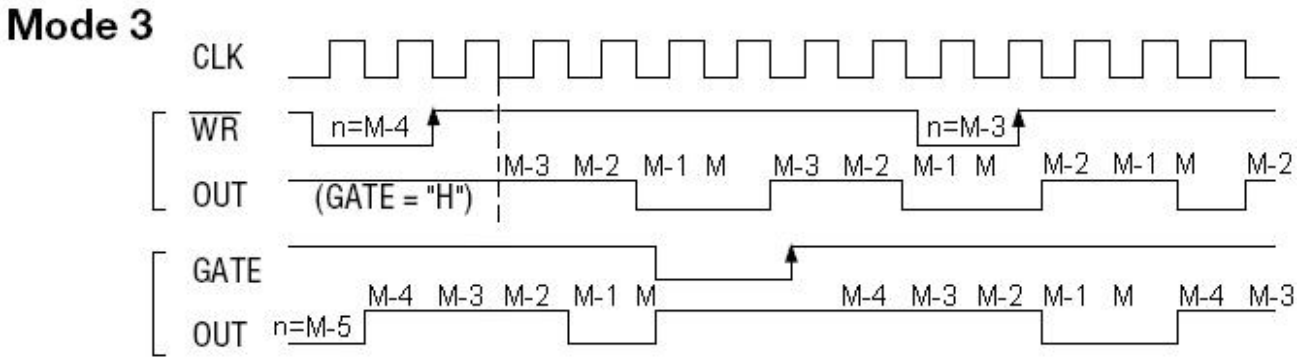


Figure 10

Mode 4: Software triggered strobe

Under this mode, the counter starts counting after is given the initial value n, and OUT becomes high level. When the count value becomes M, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting.

Time diagram is shown in figure 11.

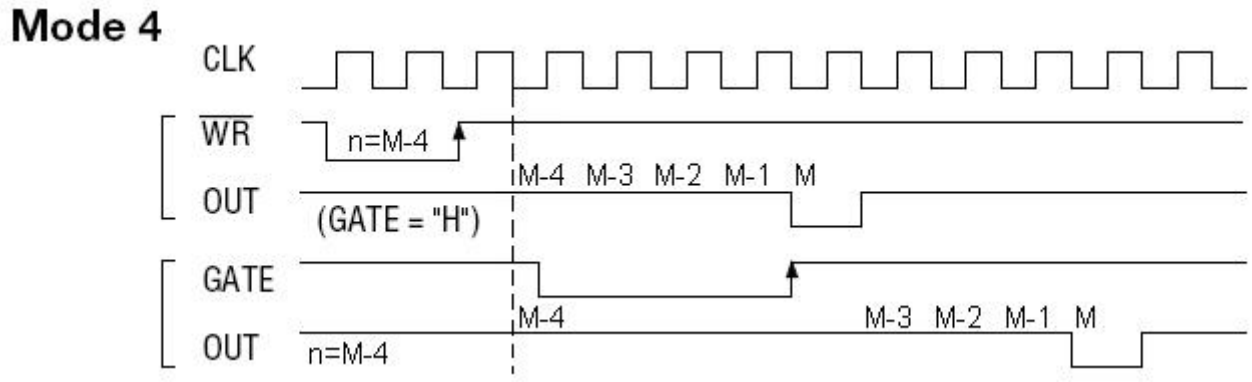


Figure 11

Mode 5: Software triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes M, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. If a counter which is counting is given a new value, it does not affect the current operation. Only when the value turns to “M” and there is a “GATE” rising edge, the counter will begin to count from the new value.

Time diagram is shown in figure 12.

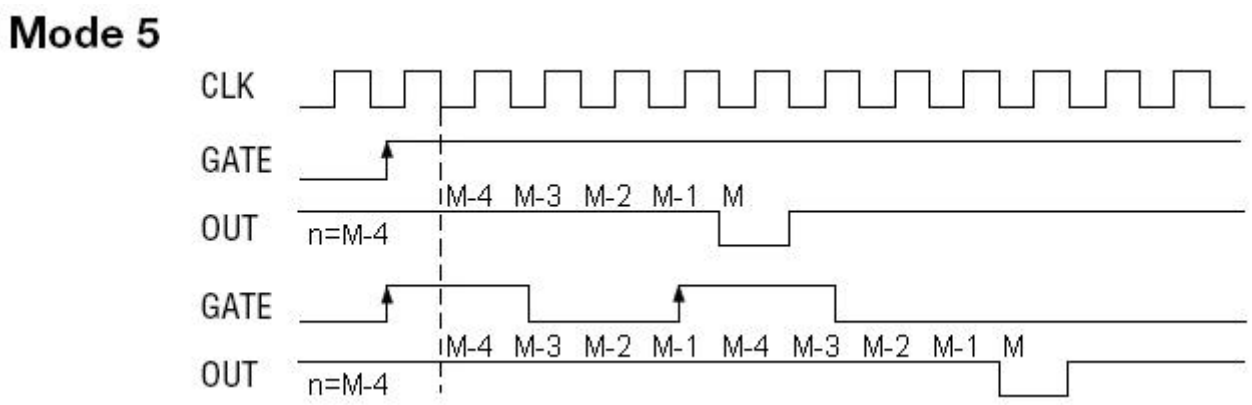

Mode 5
CLK
GATE
M-4 M-3 M-2 M-1 M
OUT
n=M-4
GATE
M-4 M-3 M-2 M-1 M-4 M-3 M-2 M-1 M
OUT
n=M-4

Figure 12

Chapter 6 Notes and Warranty Policy

6.1 Notes

In our products' packing, user can find a user manual, a PCI2390 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using PCI2390, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PCI2390 module.

6.2 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.